

As the Examiner notes, the Examiner cited "line setting processors" in the preamble as the link layer processor. Thus, the Examiner set the Examiner's context for alleging teachings as to a "method for processing ingress data units in a link layer processor" as being in "line setting processors."

Applicant notes Osaki states, at column 6, lines 31-33, "Shown in FIG. 2 is an interior structure of each of the line setting processors 108-1 to 108-n (which is represented as the typical line processor 108 in the drawing)." Moreover, line setter 211 and call setter 212 are depicted in FIG. 2. Therefore, within the context alleged by the Examiner, Applicant has presented argument concerning line setter 211 and call setter 212 as to why Osaki fails to disclose the claimed "method for processing ingress data units in a link layer processor," as recited in claim 24.

In the most recent Office action, Applicant notes the Examiner cites "Fig. 1@109, path management processor" with respect to the preamble instead of "line setting processors," as cited in the previous Office actions. Accordingly, Applicant shall address the alleged teachings within the new context alleged by the Examiner. Moreover, Applicant appreciates the Examiner's heightened specificity in identifying elements and descriptive portions of Osaki relied upon by the Examiner in alleging the rejection.

Applicant submits Osaki fails to disclose the claimed invention as set forth in claim 24. For example, Applicant submits Osaki fails to disclose "receiving a first ingress data unit corresponding to a call. The Examiner alleges "meta-signalling signal" teaches "a first ingress data unit corresponding to a call." However, as noted previously with respect to line setter 211 and call setter 212, Osaki distinguishes between "setting of a line channel" and "management of user's communication mode (which is referred to as the call...)" (col. 6, lines 64-67). As Osaki states, "meta-signalling signal 601 demand[s] the setting of the line setting signal path..." (col. 9, lines 51 and 52), Applicant submits Osaki teaches the "meta-signalling signal" relating to "line setting," not "receiving a first ingress data unit corresponding to a call. Thus, even based on the "receiving a call setup signal at the line interface, meta-signalling signal, see col. 9 lines 50-53, also see Fig. 6," as identified by the Examiner, Applicant submits Osaki fails to disclose "receiving a first ingress data unit corresponding to the call.

As another example, Applicant submits Osaki fails to disclose, "forwarding the first ingress data unit to the first selected intermediate processor." Osaki states, at col. 9, lines 51-53, "...a meta-signalling signal 601 demanding the setting of the line setting signal path is first transmitted from the terminal to the line interface 102." Osaki further states, at col 10, lines 15-21, "Subsequently, the line-setting-signal path management processor 109 transmits a signal 603 (including the signal reception

channel data from the line and the routing tag data for transmission of the line setting signals to the signal channel of the line in the illustrated example) to the determination processor by which the processing of the line is determined to be processed." Thus, Applicant submits Osaki fails to teach "forwarding the first ingress data unit...", where "the first ingress data unit" is consistent with what the Examiner asserted to teach the "first ingress data unit" with respect to "receiving a first ingress data unit corresponding to a call."

For the foregoing reasons, Applicant submits Osaki fails to teach the claimed invention as set forth in claim 24. Thus, Applicant submits claim 24 is in condition for allowance.

The Examiner has rejected claims 25 and 27, stating, "in Osaki a line setting processor is selected by the path management processor based on loading (col. 2 lines 62-66). Applicant submits Osaki fails to disclose the subject matter of claim 24, from which claims 25 and 27 depend. Therefore, Applicant submits claims 25 and 27 are in condition for allowance.

The Examiner has rejected claim 26 under 35 U.S.C. § 103(a) as being unpatentable over Osaki. However, such rejection was never raised in a non-final Office action. Rather, Applicant submits the Examiner raised this purported ground of rejection that is neither necessitated by Applicant's amendment of the claims nor based on information submitted in an information disclosure statement. Thus, Applicant respectfully requests finality of this Office action be withdrawn in accordance with MPEP § 706. Furthermore, the Examiner has not cited any reference in the prior art as disclosing "a round robin scheme." Significantly, the Examiner also has not cited any suggestion in the prior art to combine "a round robin scheme" with the teachings of Osaki. Thus, Applicant submits the Examiner has failed to establish a *prima facie* showing of unpatentability under 35 U.S.C. § 103(a) with respect to claim 26. Thus, Applicant submits claim 26 is in condition for allowance.

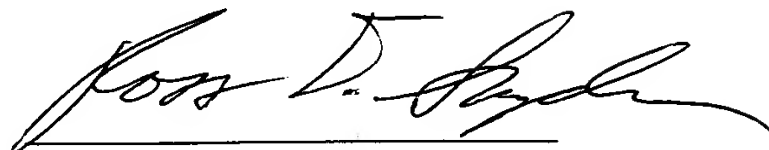
The Examiner has allowed claims 1-23. The Examiner has objected to claims 28-31 but states that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has presented arguments for the allowability of claim 24, from which claims 28-31 depend. Therefore, Applicant submits claims 28-31 are also in condition for allowance.

In conclusion, Applicant has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the

Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

07/05/2005
Date



Ross D. Snyder, Reg. No. 37,730
Attorney for Applicant(s)
Ross D. Snyder & Associates, Inc.
115 Wild Basin Road, Suite 107
Austin, Texas 78746
(512) 347-9223 (phone)
(512) 347-9224 (fax)